

**Prior Art** 

FIG. 1

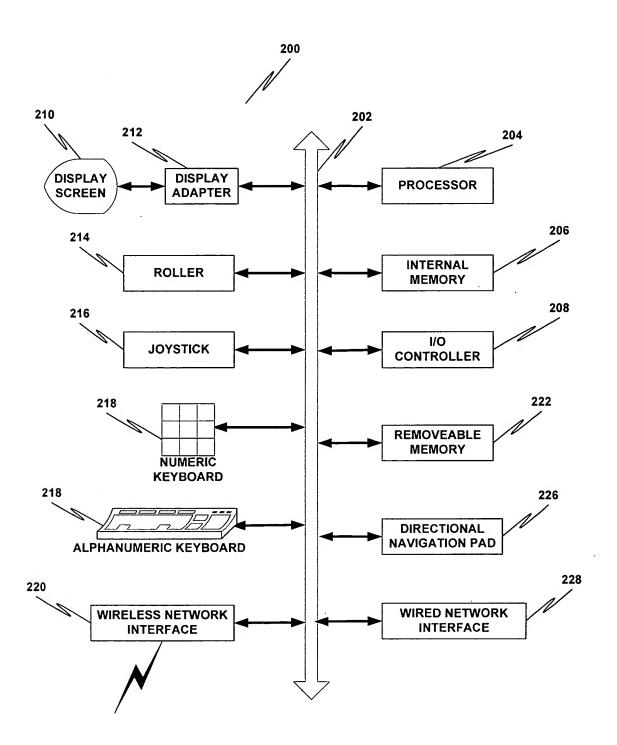
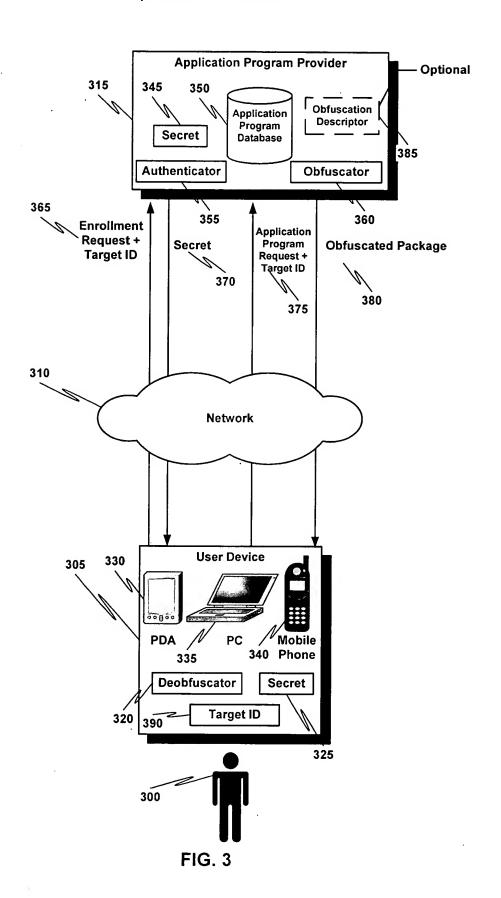
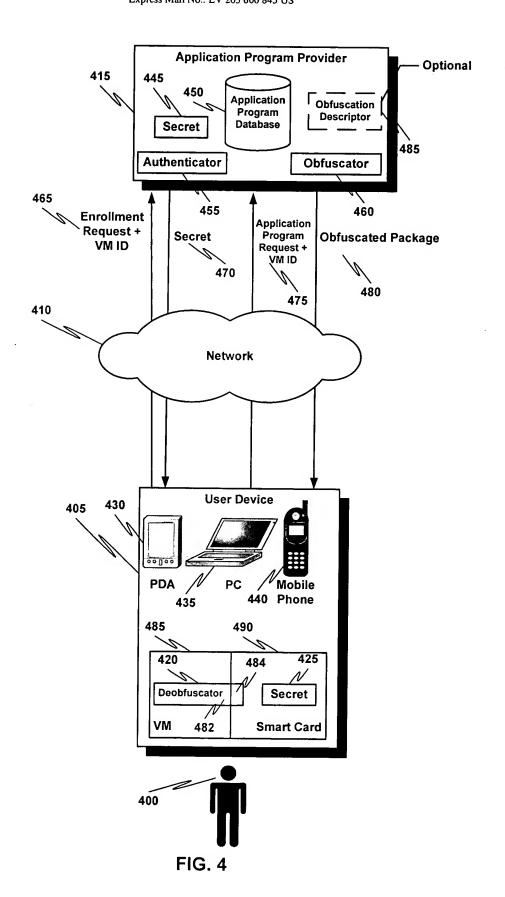


FIG. 2





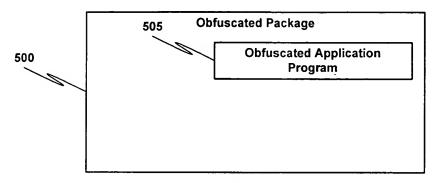


FIG. 5A

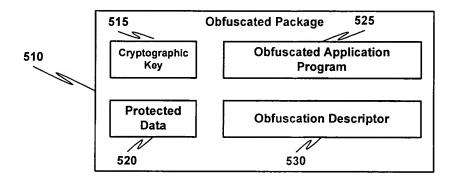


FIG. 5B

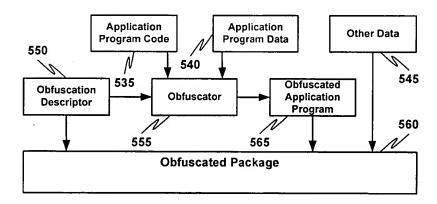


FIG. 5C

FIG. 5

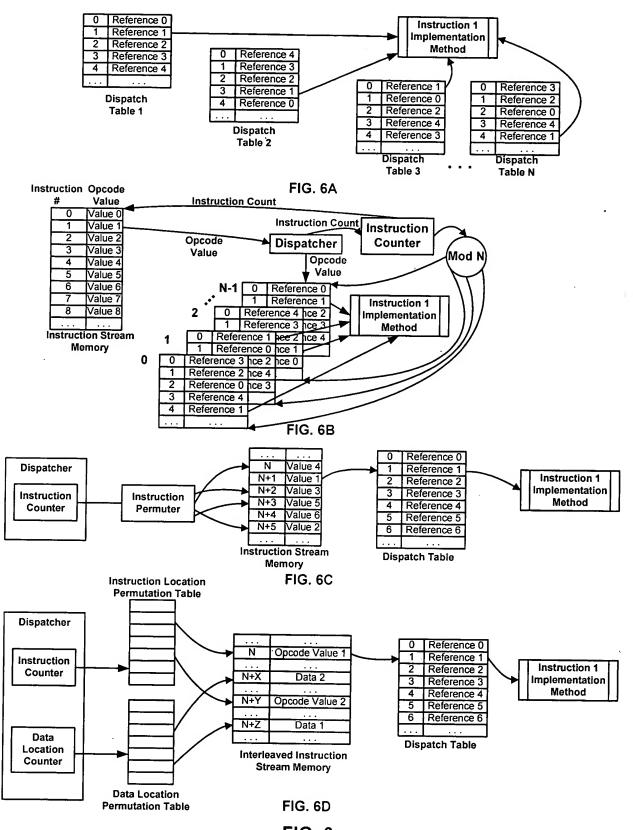


FIG. 6

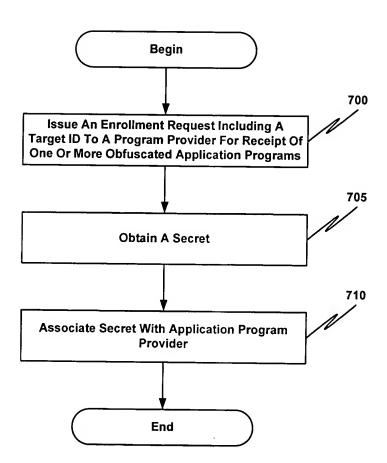


FIG. 7

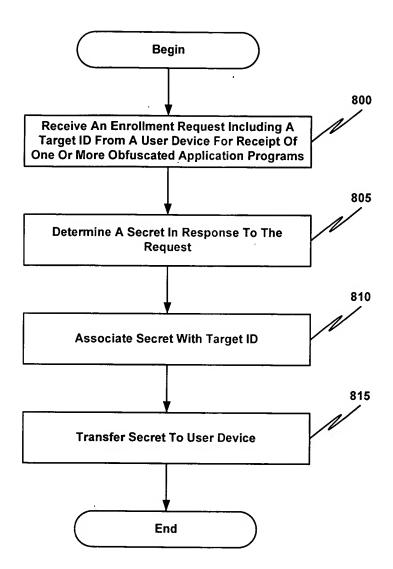
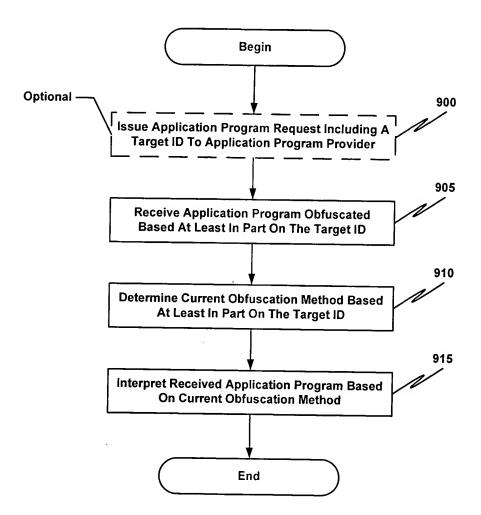
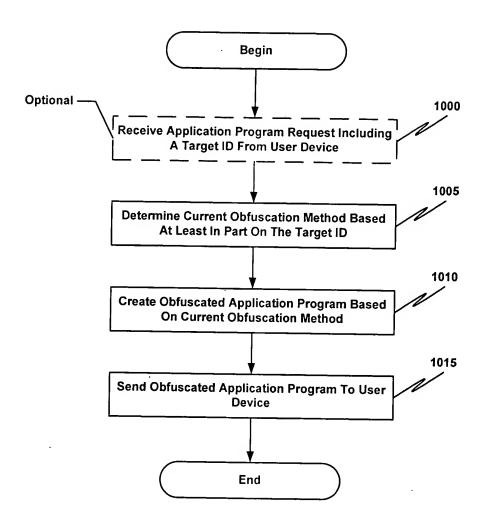


FIG. 8





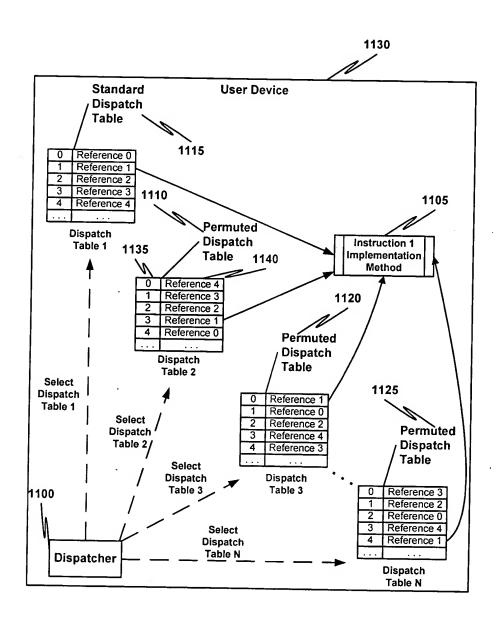


FIG. 11

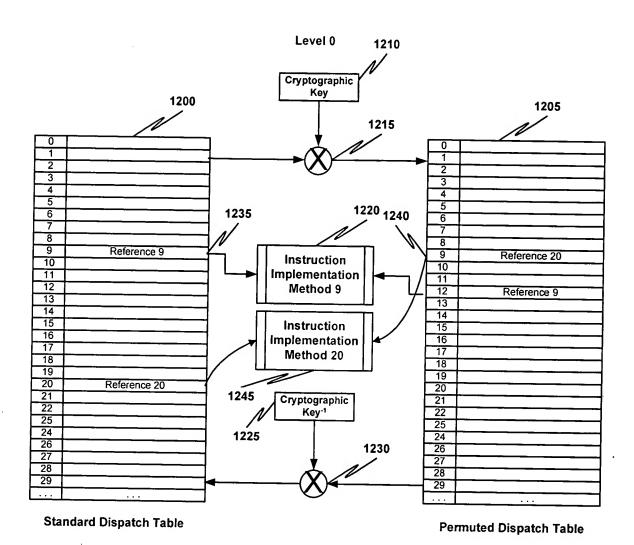


FIG. 12

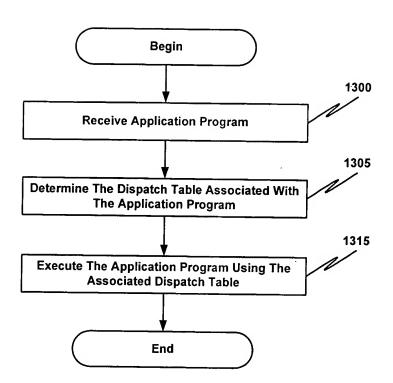


FIG. 13

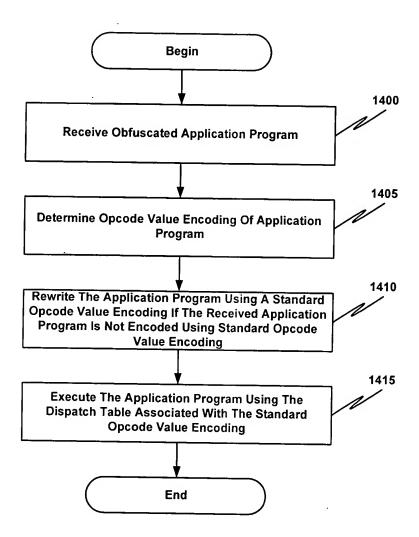
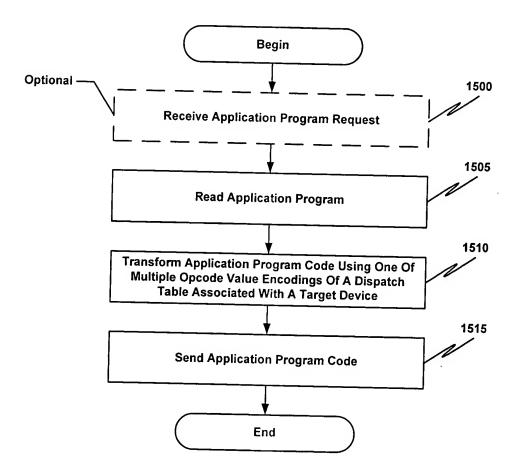
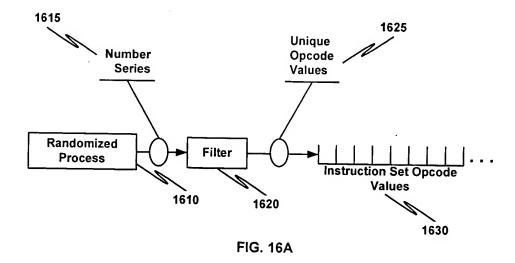


FIG. 14





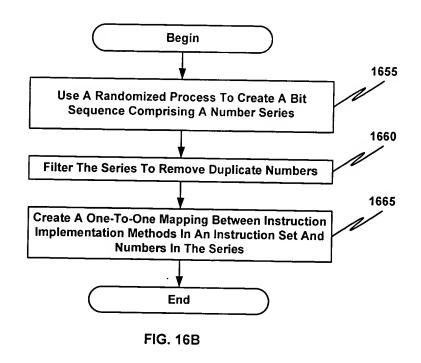
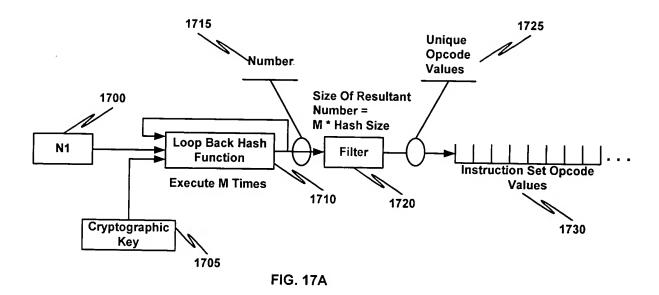


FIG. 16



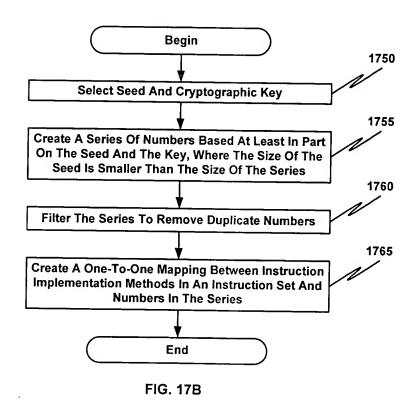


FIG. 17

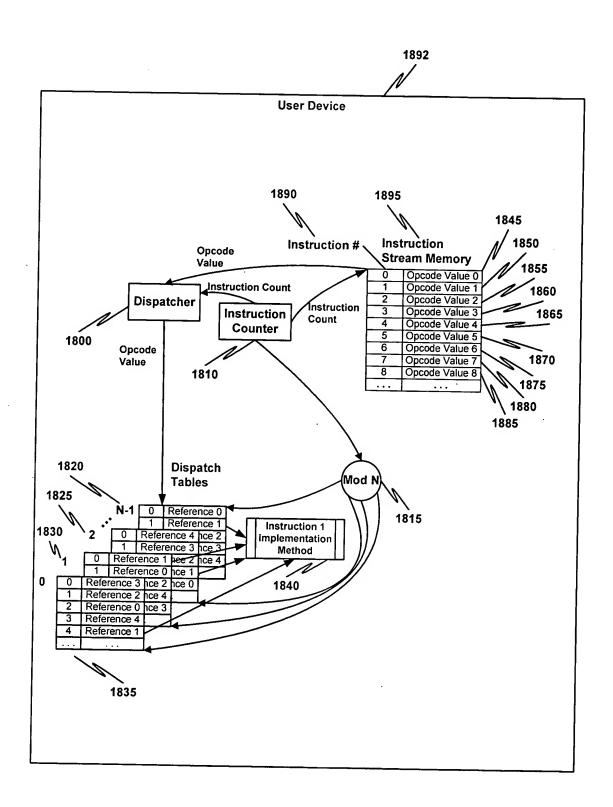


FIG. 18

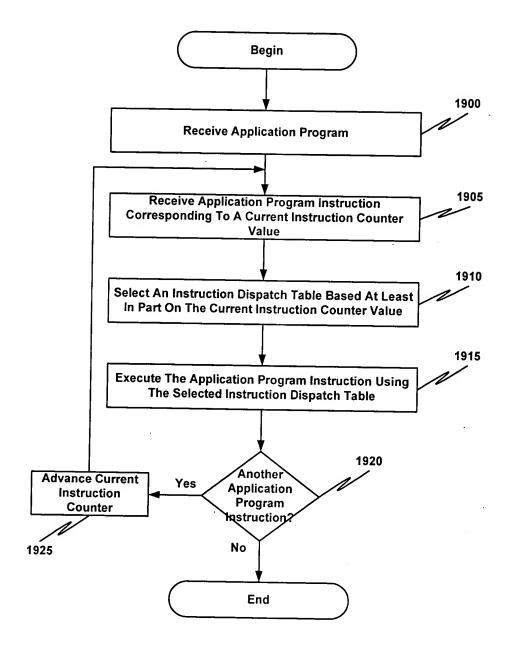


FIG. 19

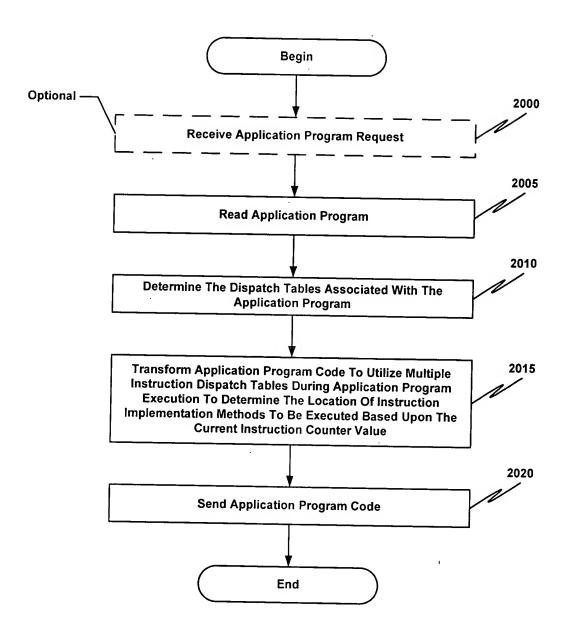


FIG. 20

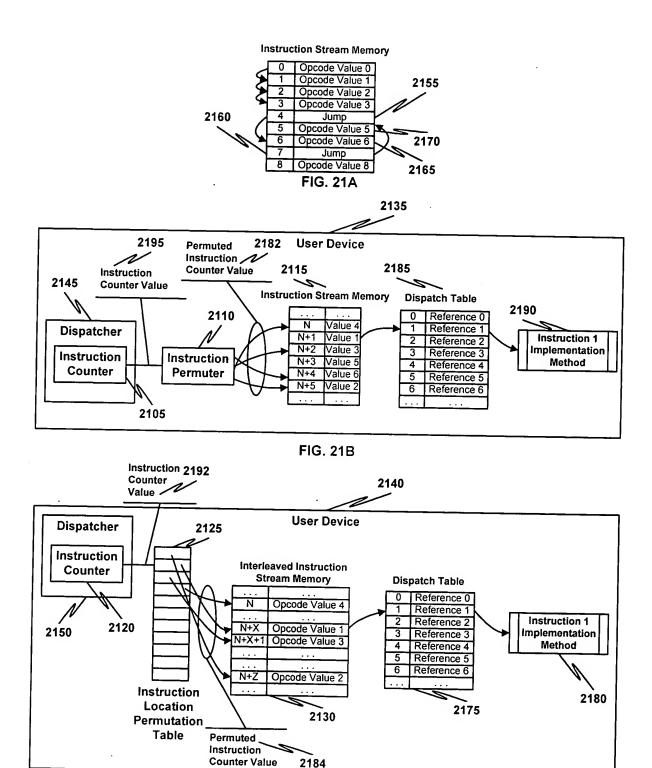


FIG. 21C

FIG. 21

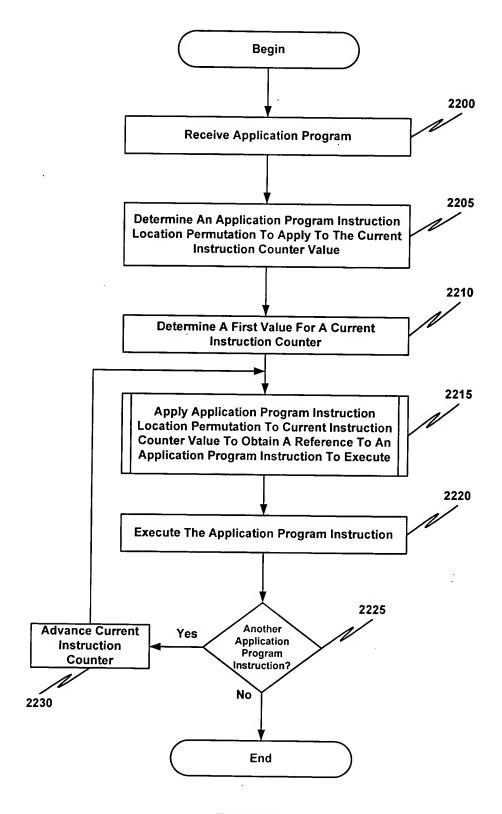


FIG. 22

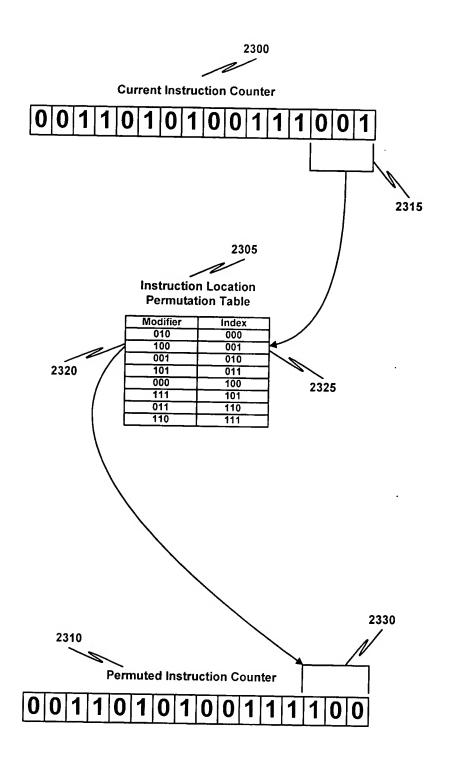
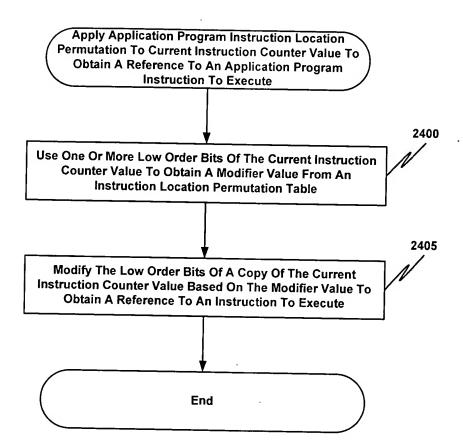
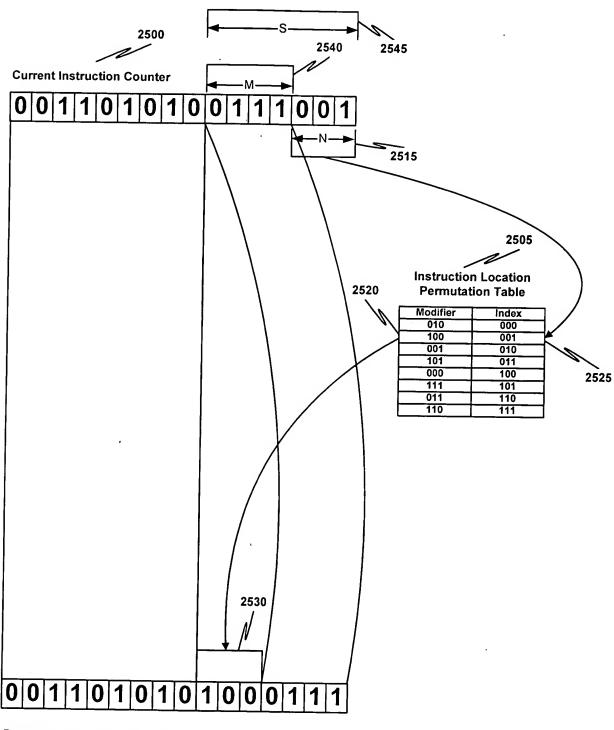
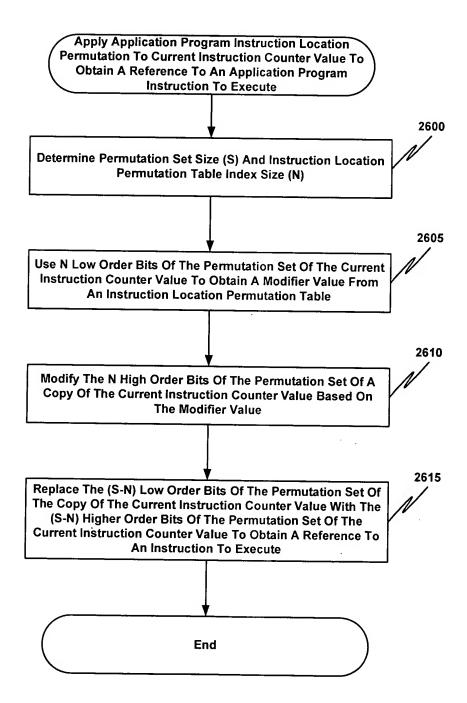


FIG. 23





Permuted Instruction Counter



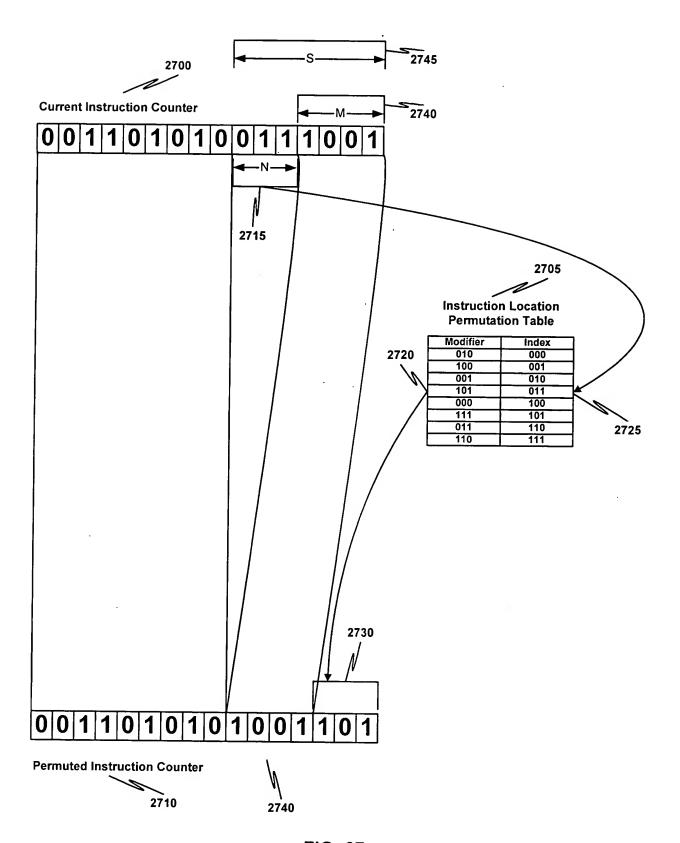
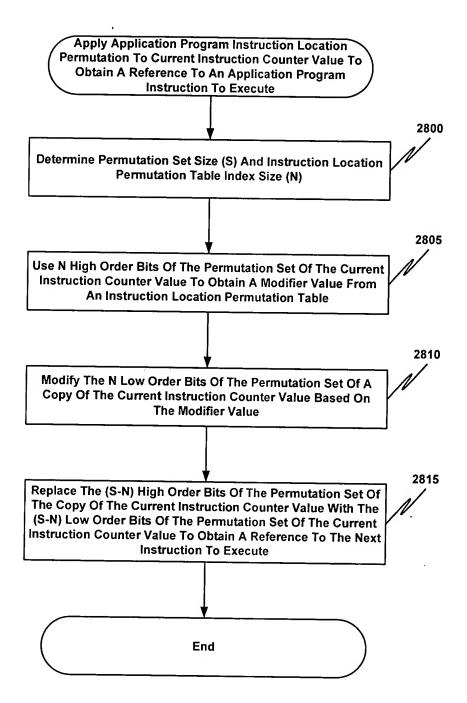


FIG. 27



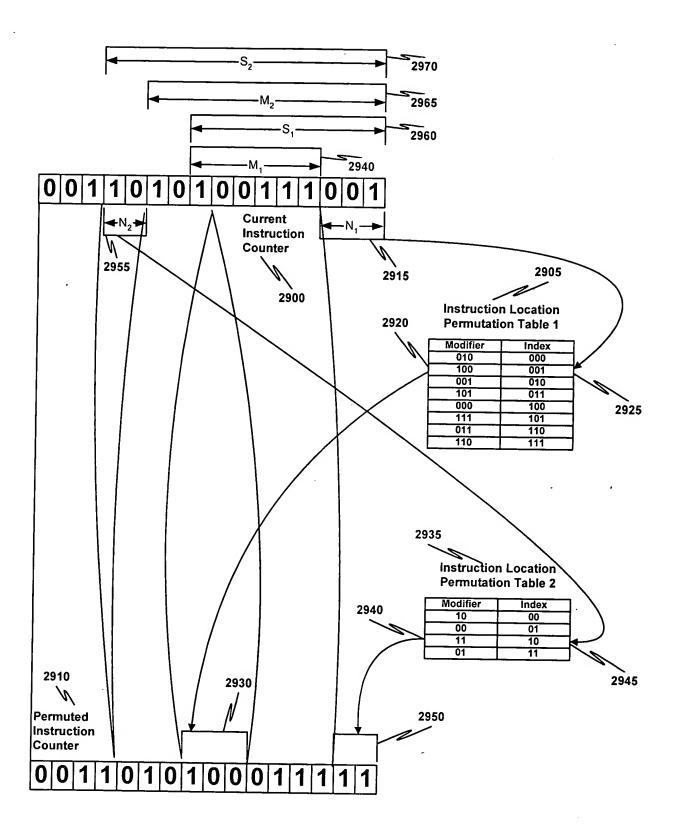
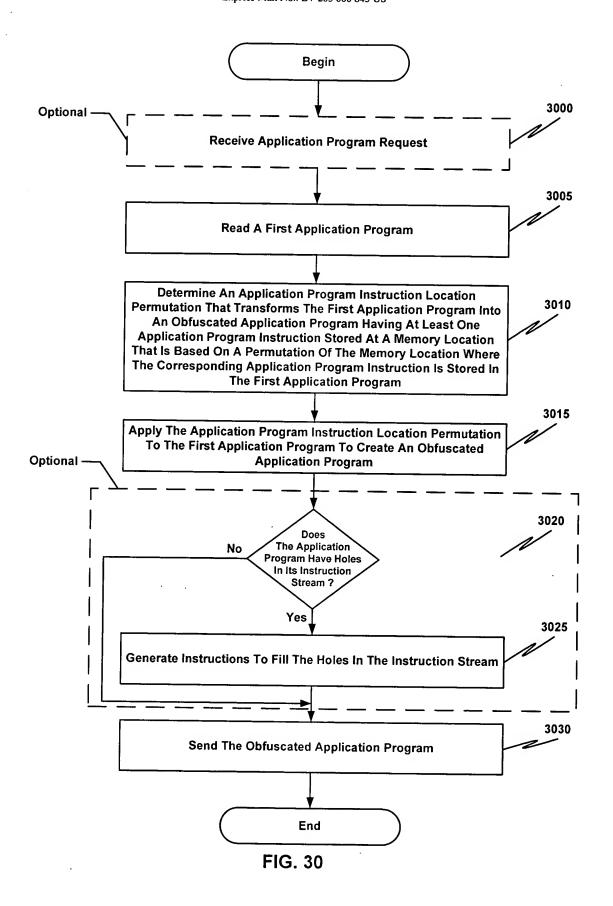


FIG. 29



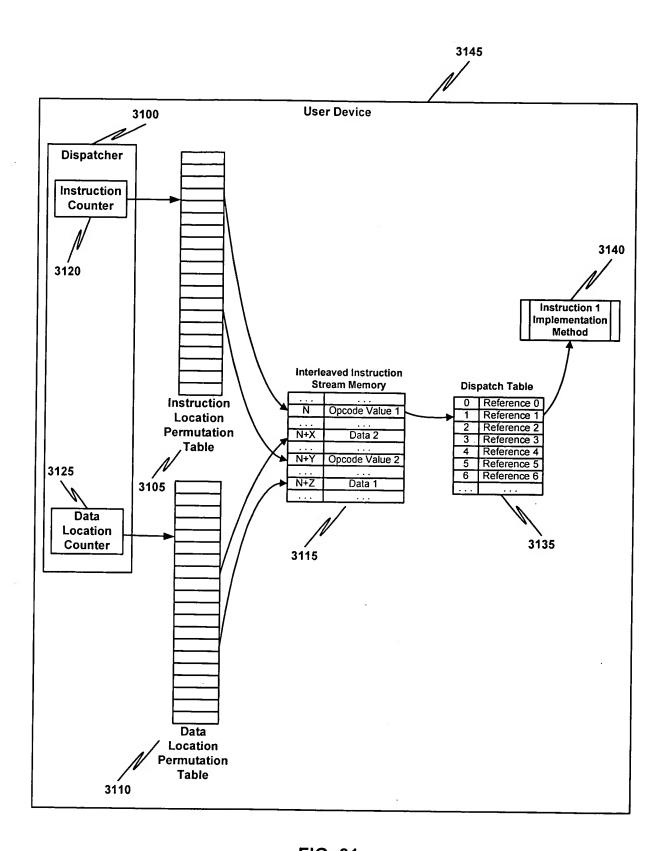


FIG. 31

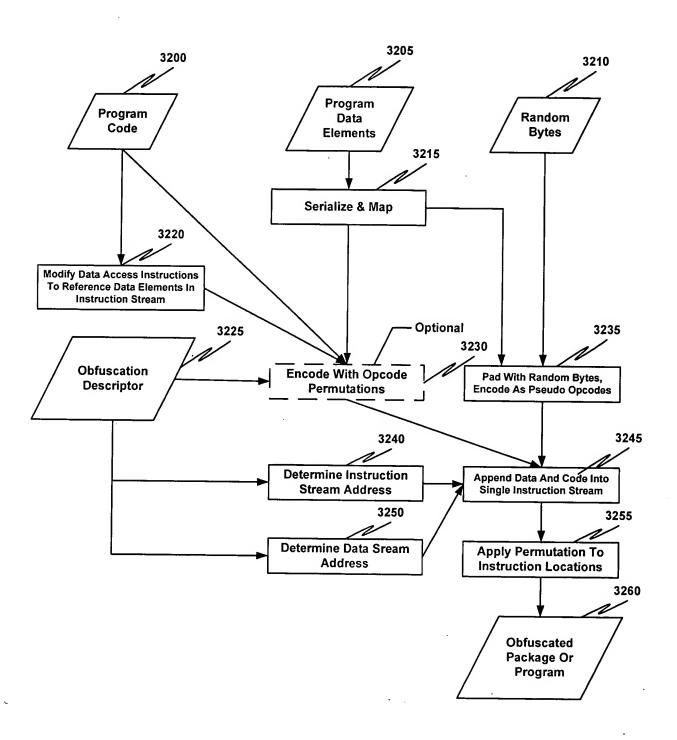
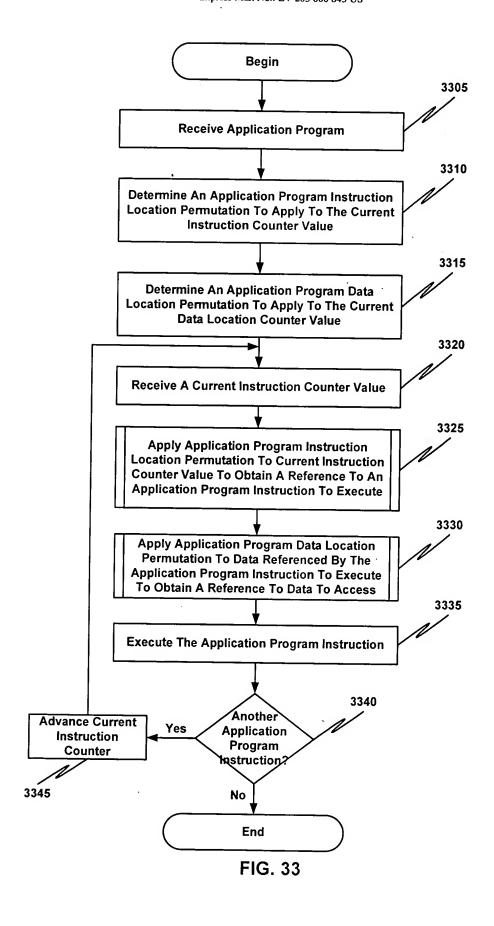


FIG. 32



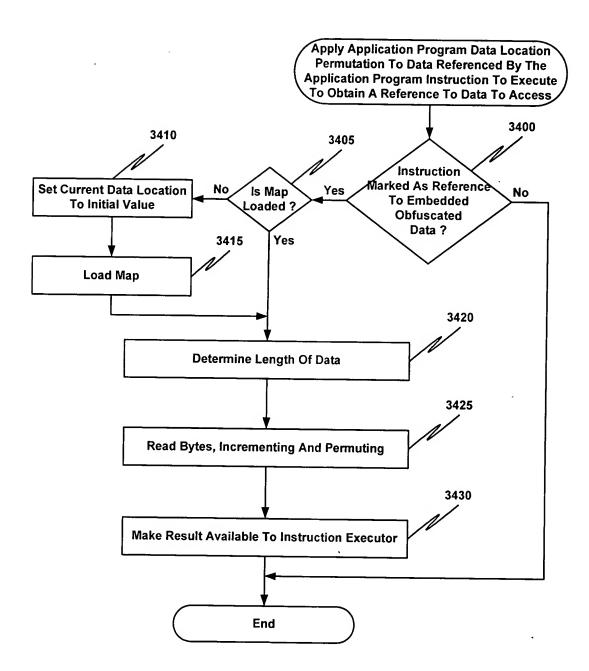
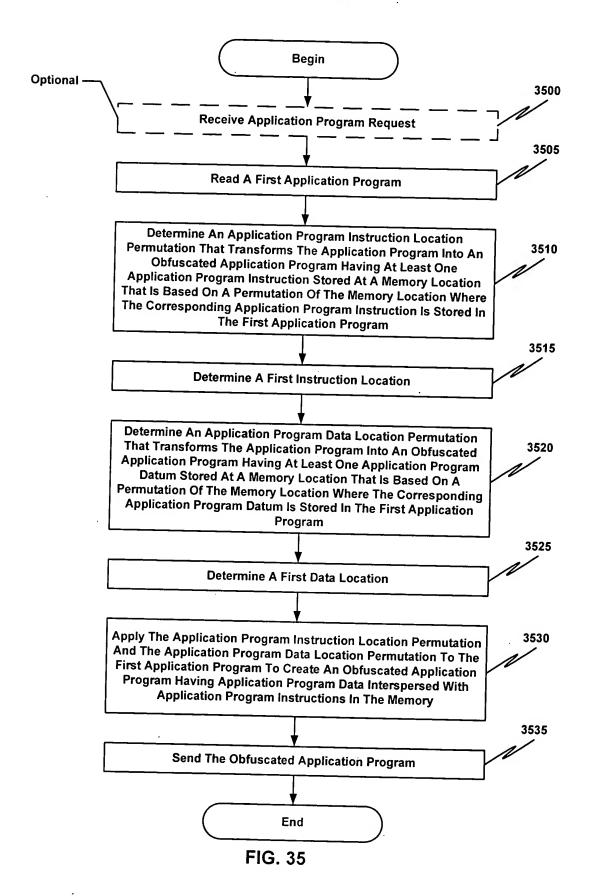


FIG. 34



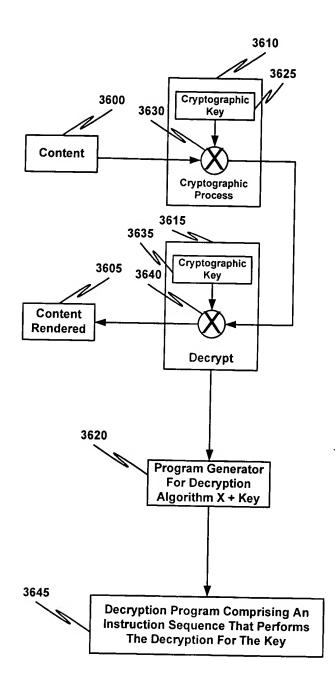


FIG. 36

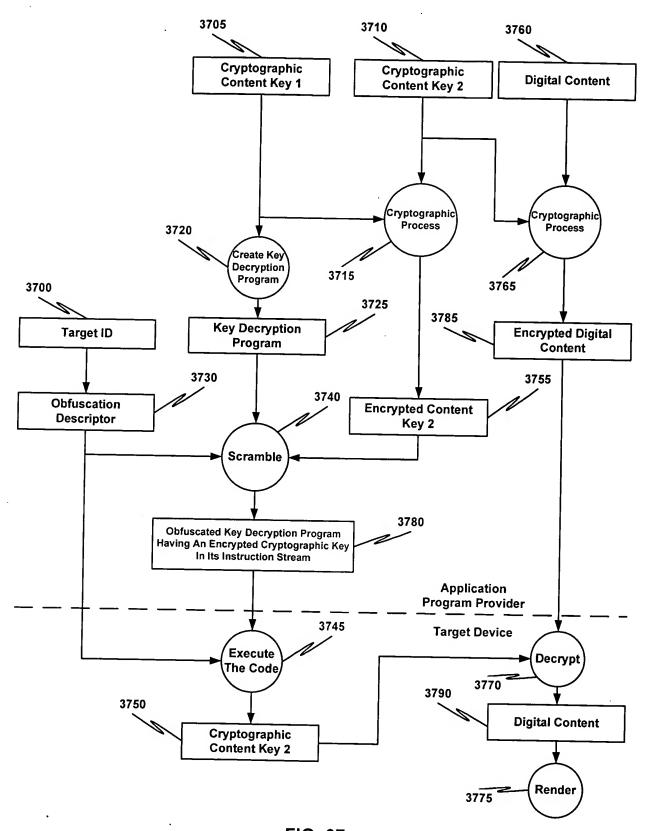


FIG. 37

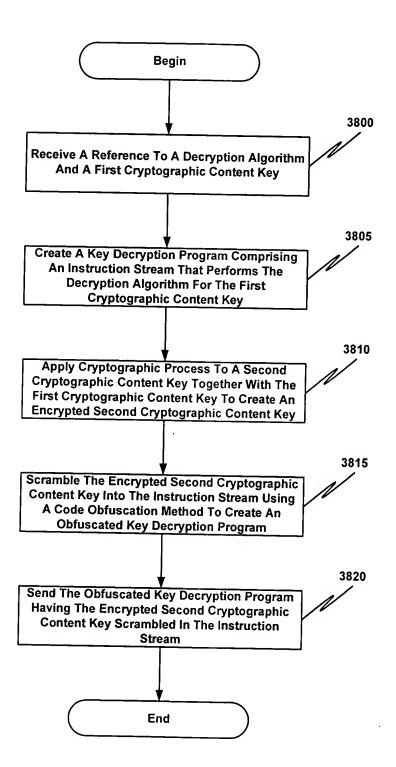


FIG. 38

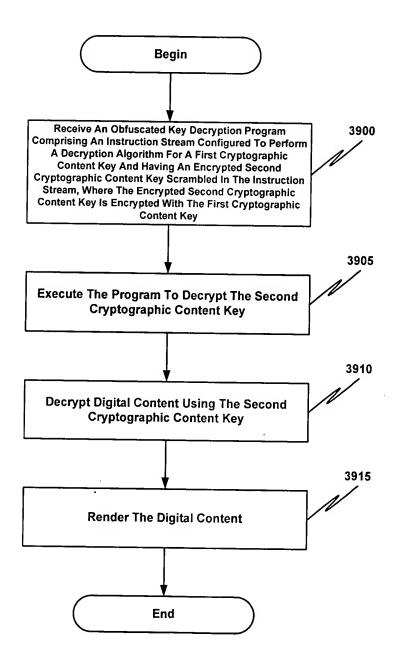


FIG. 39